UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,874	09/18/2001	Mika Salmi	874.0100.U1(US)	9941

29683 7590 10/06/2003

HARRINGTON & SMITH, LLP
4 RESEARCH DRIVE
SHELTON, CT 06484-6212

EXAMINER	
NGUYEN, LINH V	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/955,874	Applicant(s) SALMI ET AL.	
	Examiner Linh V Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *Claim 2 – 9, 11 – 13, and 15 – 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *Claim 2 – 9, 11 – 13, and 15 – 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/15/02* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Respons to Amendment

1. This office action is in response to applicant's amendment received on 8/18/03. Claim 14 has been canceled. Claim 2 – 9, 11 – 13, and 15 – 21, are pending on this application.

Response to Arguments

2. Applicant's arguments, see Under Remarks page 8 , filed 08/18/03, with respect to the rejection(s)of claim(s) 2, 5, 9, and 17 under "resampling the frequency divided signal using a flip-lop circuit that has a data input coupled to frequency divided signal and a clock input that is clocked with the output signal of Voltage Controlled Oscillator" have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kim U.S. Patent No. 6,411,699.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 4, 5, 6, 8, 9, 11 and 13, are rejected under 35 U.S.C. 102(e) as being anticipated Kim U.S. Patent No. 6,411,699.

Regarding to claim 2, Figs. 2, 5 and 10 of Kim discloses a phase locked loop (Fig. 2) comprising a phase comparator (21) generating an output signal that is used to drive a voltage controlled oscillator (26), and a modulus prescaler (28a) circuit coupled to an output of said voltage controlled oscillator (CLK), said prescaler circuit comprising an input node (See 28a) for coupling to said output of said voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by L or N (Fig. 5), an output node (PS) for outputting a frequency divided signal that is coupled to said phase comparator (Fig. 2 (21)), and a plurality of divider stages (Fig. 5 (FF2 - FF8)) coupled between the input node and the output node for dividing the input signal by N and L, and further comprising at least one resampling stage (FF1) coupled to an output of at least one of said divider stages for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal (Fig. 10), thereby reducing temporal ambiguity in the occurrence of the edges of the output signal (improvement only no metes and bounds), where said at least one resampling stage is comprised of a flip-flop (FF1) having a data input coupled to said output of said at least one of said divider stages (FF3) and a clock input node (See FF1) for being clocked with said output of said voltage controlled oscillator (CLK).

Regarding to claim 3, wherein the value of N is programmable (Col. 1 line 54).

Regarding to claim 4, wherein said flip-flop is comprised of a D type flip-flop (FF1).

Regarding to claim 5, Fig. 1 of Kim discloses a method of frequency source of a mobile station, comprising: operating a phase locked loop (Fig. 5) as part of the

frequency source to generate a signal having a desired frequency (BBS), the step of operating the phase locked loop including a step of dividing a frequency of an output signal of a voltage controlled oscillator (Fig. 2) by a predetermined amount (N, L); to generated a frequency divided signal (Fig. 2 (output of 28)) and resampling (Fig. 5 (FF1)) the frequency divided signal using a flip flop circuit (Fig. 5 (FF1)) that has a data input coupled to said frequency divided signal and a clock input that (See Fig.5 (FF8)) is clocked with the output signal of the voltage controlled oscillator to reduce jitter in the frequency divided signal (purpose only, no subject matter).

Regarding to claim 6, wherein the step of resampling operates a modulus prescaler circuit (Fig. 5) that is coupled to the output of the voltage controlled oscillator (Fig. 2), the prescaler circuit comprising an input node (Fig. 2) for coupling to the output of the voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by (Fig. 5), an output node for outputting a frequency divided signal that is coupled to a phase comparator (Fig. 2 (21)) of the phase locked loop, and a plurality of the frequency divider circuits (FF2 – FF8 of Fig. 5)) coupled between the input node and the output node for dividing the input signal by N, L, where the step of resampling is accomplished in a resampling stage (FF1 of Fig. 5) coupled to an output of at least one of the frequency divider circuits (See Fig. 5) for receiving an output signal therefrom ,and for synchronizing edges of the output signal to edges of the input signal (Fig. 10), thereby reducing jitter of the output signal (purposes or advantages or improvement only, not a subject matter for "thereby reducing jitter of the output signal").

Regarding to claim 7, wherein the value of N is programmable (Col. 1 line 54)

Regarding to claim 8, wherein said flip-flop is comprised of a D type flip-flop (Fig. 5 (FF1)).

Regarding to claim 9. Fig. 1 and 2 of Kim discloses a method to operating a phase locked loop as part of the frequency source to generate a signal having a desired frequency (BBS), comprising: operating a multi-modulus prescaler (Fig. 2 (28)) function of the phase locked loop to divide a frequency of an output signal of an oscillator by a predetermined amount (Fig. 5) to generate a frequency-divided signal; and resampling the frequency divided signal (Fig. 5 (FF1)) using a flip-flop circuit that has a data input coupled to the frequency divided signal and a clock input that is clocked with the output signal of the oscillator (CLK of Fig. 5).

Regarding to claim 11, wherein the step of resampling operates a prescaler circuit (Fig. 2 (28)) that is coupled to the output of the oscillator (Fig. 2 (26)), the prescaler circuit comprising an input node (see Fig. 2) for coupling to the output of the oscillator (CLK) for receiving an input signal having a characteristic frequency to be divided by L, N (Fig. 5) an output node for outputting a frequency divided signal that is coupled to a phase comparator (See Fig. 2 (21)) of the phase locked loop , and a plurality of the frequency divider circuits (Fig. 5) coupled between the input node and the output node for dividing the input signal by N, L, where the step of resampling is accomplished in a resampling stage (Fig. 5 (FF1)) coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal (Fig. 10), thereby

equalizing the delay added in different modes of the multi-modulus prescaler function (advantages/improvement only, not a subject matter).

Regarding to claim 12, wherein the value of N is programmable (Col. 1 line 54)

Regarding to claim 13, wherein said flip-flop is comprised of a D type flip-flop (Fig. 5 (FF1)) that is clocked with the input signal of the oscillator (CLK of Fig. 5)

Regarding to claims 15 – 16, Fig. 1 Kim teach a mobile station using the PLL circuit (Col. 1 lines 5 – 19).

Regarding to claim 17 - 21, Figs. 1, 2, 5 and 10 of Kim as applied to claims 2 – 9, 11 – 13, and 16, above disclose every aspect of applicant's claimed invention.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

September 10, 2003

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800